REMARKS

Applicants appreciate the Examiner's detailed Office Action and consideration of Applicants' claimed invention.

Applicants have amended the application as shown above to correct clerical errors and to clarify the claims and specification.

In ¶ 3, the Office Action objects to the specification at Page 15, line 27, and more particularly to the term "the controlling tty" as unclear. This term would be known to a person of skill in the art of the UNIX operating system. The term is generally used to refer to the terminal (tty) controlling a particular job in the UNIX system. The common usage of the term can be confirmed via a simple search on the Internet. Please advise Applicants if further clarification is required.

In ¶¶ 4, 5, and 6, the Office Action objects to Claims 43, 50, and 55 under 35 U.S.C. 112. In response, Applicants have deleted the misplaced phrase "Interrupt driven value sampling" after "WHAT IS CLAIMED IS:". Applicants have amended claim 50 to remove reference to the term "JAVA." Applicants have also amended claim 55 to remove the duplicative "such that" phrase. Applicants have also amended claim 43 to remove the relative term "high degree." Accordingly, Applicants submit that there is no basis for objection to the claims under 35 U.S.C. 112.

With respect to all pending claims, Claims 1-72, Applicants respectfully submit that these claims are allowable for at least the reasons set forth below:

In ¶ 8, the Office Action rejects the independent claims of the Application, Claims 1, 66, and 69 (and claims depending therefrom) under 35 U.S.C. 102(b) as being anticipated by Agrawal, US Pat. No. 5,768,500. In particular, the Office Action rejects Claim 1 (and other claims) of the patent submitting that the Agrawal reference discloses data values being stored and associated with a particular object code instruction. Specifically, the Office Action references col. 10, lines 26-34 in which Agrawal notes that a brief sampled state record may be appended to a kernel profiling buffer. *Agrawal at col. 10, lines 26-34.* "The record typically contains information such as: (Timestamp, Current Process Id, Processor Status Word, Current Program Counter Value)." *Id.* The Office Action also notes that

the "Examiner considers this type of information sufficient to associate a data value with an instruction." Applicants respectfully disagree that this is sufficient to teach the claimed elements of Applicants' invention.

As amended, Claim 1 recites in part "...storing at least one data value of interest in a first database, the at least one data value of interest being associated with a particular object code instruction of the program, the particular object code instruction being executed by the computer when the interrupt occurs...". Agrawal fails to teach this limitation.

Agrawal essentially discloses a memory system profiler that samples system state using interrupts generated by a cache miss counter, compare register, and interrupt line. *See Agrawal at col. 2, lines 37-41.* Agrawal does not contemplate nor can it accomplish the association of the data/information sampled with the particular object code instruction of the program being executed by the computer when the interrupt occurs, as is claimed by Applicants. This is a standard inadequacy in interrupt-driven sampling. This inadequacy is caused in part by latency in the interrupt handling and the potentially complex sequencing of instructions executed in a processor. (It should be noted that the latency and instruction sequencing issues are discussed in the Chrysos reference, US 6,195,748, also cited in the Office Action. *See Chrysos col. 1, line 66 – col. 4, line 64. In particular, note col. 2, lines 18-44 and col. 3, lines 29-44 of Chrysos.*) Since the data is sampled when the interrupt occurs, and since execution of the interrupted instruction has not yet been completed, the data is not associated with the particular object code instruction of the program being executed by the computer when the interrupt occurs. Typically, the profiling system of Agrawal (or other interrupt-driven profiling systems) associates the sampled data with the instruction that initiates the interrupt (as opposed to the instruction being executed when interrupt actually occurs).

In practice, latency exists between the initiation of an interrupt and the actual occurrence of the interrupt. *See Chrysos at id.* The interrupt will occur at some time after the execution of the instruction/event that actually initiated the interrupt. *Id.* Accordingly, knowing the instruction that caused the interrupt does

not identify which instruction was executed when the interrupt actually occurs. In Agrawal for example, an instruction resulting in a cache miss would cause the cache miss counter to be incremented (or decremented). *See Agrawal at col. 8, line 34 – col. 9, line 44.* The cache miss counter would then be compared to see if the counter had reached a predetermined state sufficient to generate an interrupt. *Id.* If so, the interrupt would be generated. *Id.* In the meantime, however, the execution of instructions within the processor will have proceeded. As a result, the interrupt will occur some time later than the actual instruction that caused the cache miss and generated the interrupt.

This latency may or may not be significant for purposes of the particular system profiling and sampling being performed. For example, in Agrawal the latency may not significantly impact the profiling and analysis relating to cache misses where the data being sampled is still available and useful even though the data is not being sampled at the exact instruction which caused the cache miss. The latency, however, does prevent the simple association of the sampled data with the particular instruction being executed at the time the sampling occurs. In particular, the profiling system of Agrawal (or other interrupt-driven profiling systems) cannot simply assume that the instruction that generated the interrupt is the same instruction that was being executed at the time the interrupt occurs.

The Office Action presumes that the information/parameter that Agrawal says may be appended with the sampled data (i.e., Timestamp, Current Process Id, Processor Status Word, Current Program Counter Value) would be sufficient to identify the instruction executed and thus associate the sampled data with that instruction. This is not accurate. Of these parameters, perhaps the Current Program Counter Value (PC) would be most instructive to consider. The PC gives a return address/location for resuming the interrupted program. Essentially, the PC tells you where to go next. The PC does not, however, tell you where you came from, i.e., the instruction(s) just completed. In addition, one cannot simply decrement the PC to determine the last instruction executed (due at least in part to the out-of-order processing and branching noted above). Accordingly, these

parameters are insufficient to determine the executed instruction to which the sampled data would be associated.

Accordingly, Applicants submit that Claim 1 and the claims depending therefrom (Claims 2-65) are allowable over Agrawal. Additionally, independent Claims 66 and 69 as amended (and the claims depending therefrom, Claims 67-68, 70-72) are also allowable over Agrawal for at least the reasons discussed above.

In ¶ 10, the Office Action rejects the independent claims of the Application, Claims 1, 66, and 69 (and claims depending therefrom) under 35 USC 102(e) as being anticipated by Chrysos, US Pat. No. 6,195,748. Applicants respectfully disagree that this is sufficient to teach the claimed elements of Applicants' invention.

As amended, Claim 1 recites in part "...wherein the particular object code instruction of the program remains unmodified." Agrawal fails to teach this limitation.

Essentially, Chrysos presents a system having additional hardware apparatus, which allows for the sampling of data associated with a particular instruction. Chrysos teaches selecting a particular instruction to be sampled, augmenting the instruction to indicate its selection, and then collecting data associated with the instruction as the instruction progresses through the execution pipeline. *See Chrysos at col. 17 lines 29-43.* The data can then be sampled and stored upon completion of the execution of the particular instruction. *Id.* The selected instruction is augmented by the addition of a sample field or bit to identify the instruction during execution for sampling. *See Chrysos at col. 9, lines 17-20 and col. 13, lines 31-37.* Additional system hardware is also required to accomplish this real-time storage and sampling of data during execution of the selected instruction. *See Chrysos at Claim 1 (claiming "each of the selected instructions being augmented to indicate its selection..." and "sampling hardware capable of sampling selected instructions..." and "profile storage associated with and recording sampled information for each of the selected instructions...").* The additional system hardware comprises sampling or profiling hardware (*see col. 8,*

lines 13-15, col. 10 lines 4-5, and Figures 1, 2a and 2b) as well as profile memory/storage (*see col. 11, lines 39-46*). Applicants' invention, on the other hand, does not require augmenting system hardware or the particular selected instructions. This allows Applicants' invention to be used on legacy computer systems.

Accordingly, Applicants submit that Claim 1 and the claims depending therefrom (Claims 2-65) are allowable over Chrysos. Additionally, independent Claims 66 and 69 as amended (and the claims depending therefrom, Claims 67-68, 70-72) are also allowable over Chrysos for at least the reasons discussed above.

In ¶¶ 11-12, the Office Action also rejects Claims 15, 16-21, 42-44, 48-50, 55-57, 64-65, 67, and 71 under 35 USC 103 as being unpatentable over Agrawal and/or Chrysos in view of various combinations of the Dean, Griesemer, Salas and Gibbons references. Applicants respectfully submit that these rejections must also be withdrawn in view of the distinctions of Applicants' claimed invention over the Agrawal and Chrysos references discussed above.

Accordingly, Applicants respectfully request reconsideration and allowance of the pending claims. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned.

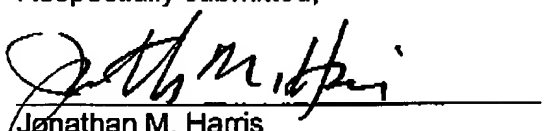
In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art that have yet to be raised, but which may be raised in the future.

If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-

Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



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